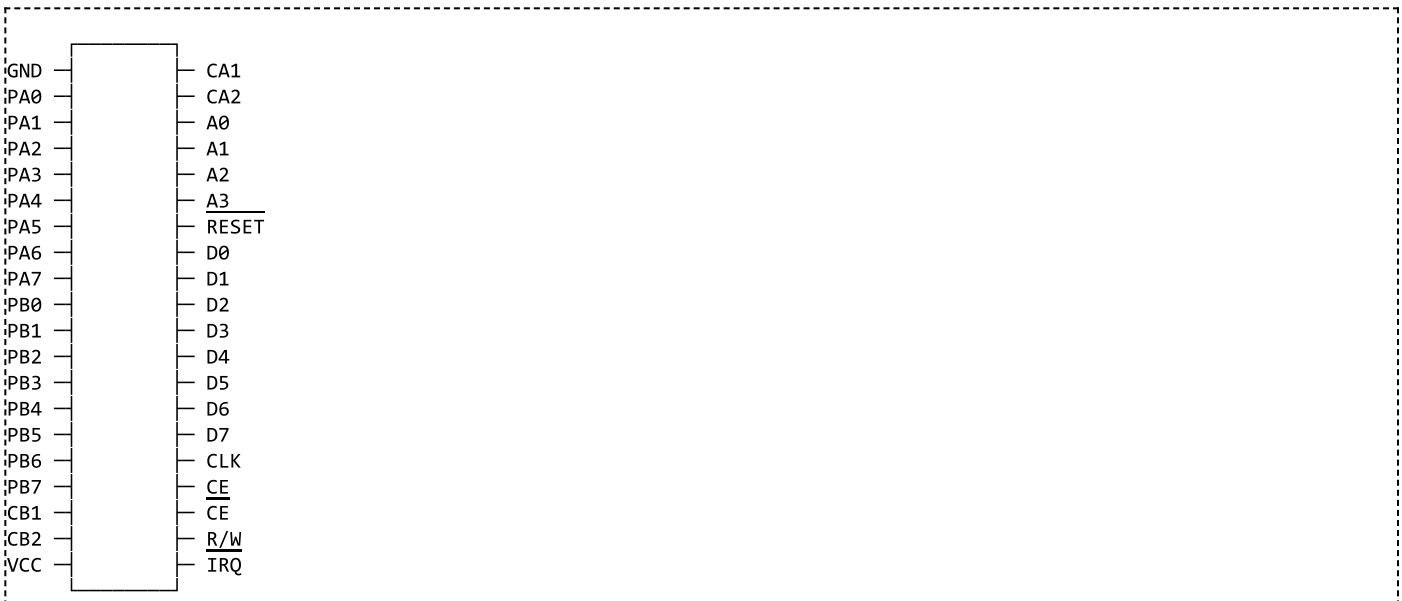
Versatile Interface Adapter

The **Versatile Interface Adapter** (known as **VIA** or **MOS Technology 6522**) is the I/O port IC used in the VIC-20. The VIA provided sixteen individually programmable I/O lines which could be read or set using bitwise instructions, and these lines were latched when in output mode. Four additional "control" lines exist: two (CA1/CB1) can be set to a constant or strobing output, or multiple input modes that trigger an interrupt; the other two (CA2/CB2) are interrupt triggers only. The VIA also included two sixteen-bit timers and an eight-bit shift register.

The VIA is still produced in CMOS by Western Design Center. It had replaced the MOS 6520 Parallel Interface Adapter used in the Commodore PET, and was replaced by the MOS 6526 Complex Interface Adapter used in the Commodore 64.

Contents

Pinout



PA0-7, PB0-7: I/O ports
CA1-2, CB1-2: Control lines
A0-A3: Address lines, connected to processor address lines A0-A3
D0-D7: Data lines, connected to processor data lines
CLK: Clock
CE: Chip enable, attached via circuitry to processor address lines A4-A5 and bank select line for the $9000 range
R/W: Read/write select for registers
IRQ: Interrupt request; connected to the 6502's Interrupt request line (VIA #2) or Non-maskable interrupt line (VIA #1)

Memory addresses

The VIA has sixteen registers, selected via the address lines. Since two VIAs are used in each VIC-20, there are two memory locations for each register.

- $9110/$9120: Port B, bitwise operations for the eight separate lines
- $9111/$9121: Port A
- $9112/$9122: Port B data direction
- $9113/$9123: Port A data direction
- $9114/$9124: Timer 1 low byte
- $9115/$9125: Timer 1 high byte & counter
- $9116/$9126: Timer 1 low byte
- $9117/$9127: Timer 1 high byte
- $9118/$9128: Timer 2 low byte
- $9119/$9129: Timer 2 high byte
- $911A/$912A: Shift register
- $911B/$912B: Auxiliary control register
  - Bits 0-1: Port A and B latch enable
  - Bits 2-4: Shift register control
    - 0 0 0 Disabled
    - 0 0 1 Shift in under control of T2
    - 0 1 0 Shift in under control of PHI2
    - 0 1 1 Shift in under control of external clock
    - 1 0 0 Shift out free running at T2 rate
    - 1 0 1 Shift out under control of T2
    - 1 1 0 Shift out under control of PHI2
    - 1 1 1 Shift out under control of external clock
  - Bit 5: Timer 2 control (0 = Timed interrupt; 1 = Count down with pulses on PB6)
  - Bits 6-7: Timer 1 control
    - 0 0 Timed interrupt each time T1 is loaded; PB7 disabled
    - 0 1 Continuous interrupts; PB7 disabled
    - 1 0 Timed interrupt each time T1 is loaded; One shot output
    - 1 1 Continuous interrupts; Square wave output
- $911C/$912C: Peripheral control register
  - Bit 0: CA1 control (pos/neg trigger)
  - Bits 1-3: CA2 control
    - 0 0 0 Input-negative active edge
    - 0 0 1 Independent interrupt input-negative edge
    - 0 1 0 Input-positive active edge
    - 0 1 1 Independent interrupt input-positive edge
    - 1 0 0 Handshake output
    - 1 0 1 Pulse output
    - 1 1 0 Low output
    - 1 1 1 High output
  - Bit 4: CB1 control
  - Bits 5-7: CB2 control
- $911D/$912D: Interrupt flag register
- $911E/$912E: Interrupt enable register
- $911F/$912F: Port A output

Physical connections

The two VIAs were attached to various devices on the VIC-20:

VIA 1 ($9110-$911F)

- PA0-1: Serial port
- PA2-4: Joystick
- PA5: Light pen
- PA6: Cassette switch
- PA7: Serial port
- PB0-7, CB1-2: User port*
- CA1: Keyboard RESTORE key
- CA2: Cassette motor

VIA 2 ($9120-912F)

- PA0-PA7: keyboard row
- PB0-PB7: keyboard column
  - Some joystick port connections are also wired into the keyboard matrix
- CA1: Cassette port write
- CA2, CB1-2: Serial port

* While PB and CB lines are the primary user port interface and are attached to the bottom side of the user port, the various functions on the PA lines are also attached to the top of the user port.

External links

http //www westerndesigncenter com / wdc/w65c22-chip.cfm